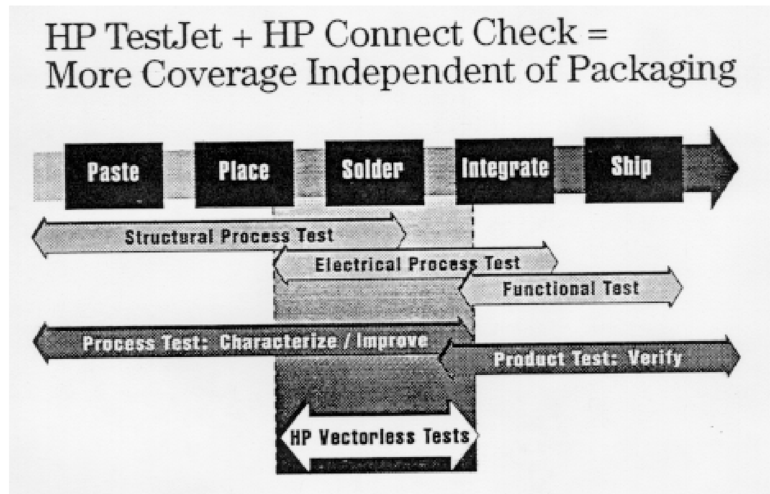
Reducing Process Defect Escapes with Vectorless Test



Process defects that escape in-circuit test lead at best to increased repair costs, and at worst to a “bone pile1" problem. The test engineer's primary goal is to pass good boards (and fail bad boards) as fast as possible within time and budget constraints. The way to achieve that goal is to:

1. Be sure the test covers the defects most likely to occur.
2. Allow as few escapes as possible. Two typical, technical causes of escapes (or false passes) out of board test can be mitigated:
    a. Maximize test coverage for a device (e.g., adjust for packaging interference).
    b. Choose an appropriate test technique for optimal results.

Test strategy determines the test coverage, test development time, maintenance time and fixture costs. The test technique determines its specific strengths and limitations in passing only good boards and failing only bad boards.

While many factors influence test strategy, time and budget constraints are important drivers. Test engineers must look for reliable, effective test techniques with:

- lower overall costs;
- less time required to develop, implement and maintain them; and
- good test coverage.

This has led to increased interest in vectorless test solutions, which can meet all of these criteria for certain kinds of defects.

1. Effectiveness Be Sure The Test Covers The Defects Most Likely To Occur The first step to effective testing is to be sure the test technique addresses the defects most likely to occur. In the shift to surface

mount technology (SMT), manufacturers have observed a shift in their fault spectrum from solder shorts to increased solder opens. In fact, the problem might be even more pervasive than is obvious. Recent discussions with manufacturers suggest that up to half of the "faulty component" diagnoses they received at functional test were actually due to undiagnosed solder opens not bad parts.

1 "Bone Pile" is an accumulation of defective boards which escape detection and which now may be too costly to diagnose and repair. Some call their bone pile "work in progress," "overhead," "scrap," or "write-off."

2 Conversations between Hewlett-Packard's Manufacturing Test Division staff with global manufacturers, Feb-May 1996

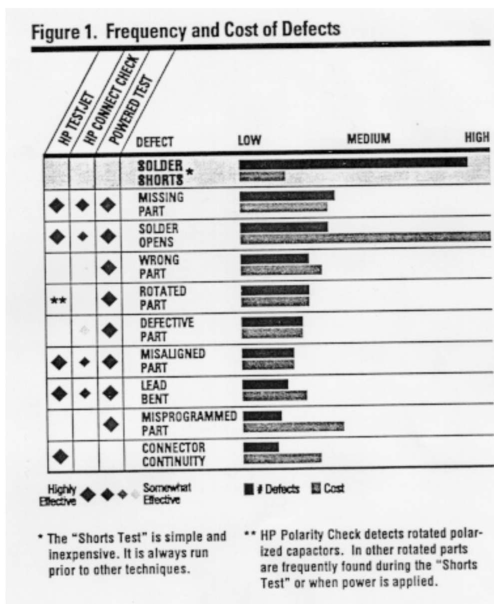
Figure 1 shows relative frequency and cost of typical SMT defects, and the effectiveness of three possible techniques for detecting them.

While powered tests can find opens, they require much detailed information and a long time to program, time that is simply no longer available with today's compressed time-to-market demands. The advent of vectorless test has made it possible to diagnose solder opens to the pin level -- lowering the number of escapes -- early in the manufacturing .process, where repair is least expensive.

Agilent's introduction of Agilent TestJet technology in the early 1990's allowed SMT manufacturers the ability, for the first time, to quickly identify solder open defects to the pin level without the expensive, time consuming task of writing vectors and libraries for powered test. It provided a stable, reliable and transportable opens test. Yet despite its many advantages, even Agilent TestJet cannot test all packaging configurations.

2a. Maximize Test Coverage

Are All Vectorless Tests Created Equal? Simply answered, no all vectorless tests are not created equal. Different vectorless techniques depend on different factors to determine if a circuit board defect is present. Each technique has unique test coverage capabilities and inherent limitations.



Agilent TestJet revolutionized the test industry with its capacitive technique that achieves unmatched stability and reliability. By its nature, however, it cannot test certain physical configurations, such as devices with a ground plane or ceramic ball grid arrays. The rapid evolution of SMT has dramatically impacted testing of circuit boards. It is now physically possible to increase board population density, decrease pitch, and address heat challenges with this new component packaging. Agilent TestJet has responded to high-population, fine-pitch test challenges with fine-point probes, improved contact and durability. To supplement the proven benefits of Agilent TestJet technology, Agilent Connect Check was introduced.

Agilent Connect Check is a parasitic diode detection technique first patented by Hewlett-Packard in 1987. However, it was abandoned at the time in the interest of the more reliable Agilent TestJet. The parasitic diode technique is most useful when some test coverage is better than no test coverage because of packaging constraints. Its advantage is that its effectiveness is not limited by ground planes or ceramic packaging. It thus addresses those few but important situations physically inaccessible to Agilent TestJet's capacitive technique.

To achieve maximum vectorless test coverage, use both Agilent TestJet and Agilent Connect Check. Figure 2 shows which vectorless technique provides better coverage for typical board devices.

Together, Agilent TestJet + Agilent Connect Check provide wider test coverage than either technique alone, and make Agilent's vectorless test coverage independent of packaging technologies. 2b. Choose An Appropriate Test Technique For Optimal Results
Understand Inherent Technique limitations Because the vectorless techniques are based on different theoretical models, they have different abilities to detect faults, and they require different levels of effort to implement and maintain them. Both are important factors when selecting vectorless techniques.

False Pass Rate

Figure 2. Device Coverage by Technique

Device Coverage	HP TestJet (capacitive technique)	HP Connect Check (parasitic diode technique)
Devices with an internal lead frame (most digital and hybrid devices)	●	
Ball Grid Arrays (BGA) (except ceramic and stadium package)	●	
Ceramic BGAs (CBGA)		●
Stadium package BGA		●
PGA without internal ground plane	●	
PGA with internal ground plane		●
Connectors, sockets, switches	●	
Devices with grounded heat sink		●
Flip-Chips and Chip-On-Board (COB)		●
Quad Flat Packs (QFP)	●	
Small Outlines (SO)	●	
Plastic Leaded Chip Carriers (PLCC)	●	
Polarized capacitors	●	

A false pass is a fault that escapes detection during test and is passed along to the next stage of assembly and test. False pass rate is important because defective units escaping into subsequent test stages increase rework costs (by 6X or more at each next stage) and can create what is sometimes called a "bone pile." (See "The Bone Pile Phenomenon," below.)

Agilent TestJet technologies is unique among vectorless test technologies in measuring circuit-board-to-lead-frame continuity, by capacitively coupling to the lead frame of the device. Agilent TestJet does not rely on what is inside the die, so measurements are based on mathematically calculated, fixed thresholds that allow the tester to discriminate between good and bad solder joints. This means that vendor-to-vendor or lot-to-lot variations do not affect Agilent TestJet's stability and reliability. By depending on mechanically specified parameters - i.e., the area of the lead frame - Agilent TestJet ensures its stability and reliability. Agilent TestJet consistently passes good boards and fails bad boards, with a very low false pass rate.

In comparison, the parasitic diode technique (Agilent Connect Check) checks circuit-board-to-I/O-pin continuity by measuring the current through a common substrate resistance between a pair of I/O pins. None of the measured characteristics is made to specifications. There are widely different diode characteristics, vendors, device types, and batches; and based on board topology. Standard pass -- fail thresholds become very difficult to set. These challenges are addressed through a learned threshold" technique, but this too has drawbacks.

The Bone Pile Phenomenon The manufacturing process is not perfect hence some percentage of products will

have defects. Defects which are not caught (which escape) during earlier test steps are usually caught at functional test, when the product simply does not work. Functional test determines primarily whether the product can or cannot ship. It is not capable of pinpoint diagnosis of why the product cannot ship.

Most electronics manufacturers collect a ”bone pile" at the end of their manufacturing process -- an accumulation of defective boards or products which “escaped" detection and which now may be too costly to diagnose and repair. Some bone piles become embarrassingly large, filling large storerooms and empty offices. Manufacturers can compensate for the bone pile phenomenon by building more product-or by reducing the cause of the bone pile.

Ideally, the process defects would all be captured by board test, where pin-level diagnosis, or "isolation,” can easily be made. Defective units escaping into functional test increase rework cost (by 6X or more) and create the bone pile. If process defects are not detected and diagnosed at board test, they can lead to a growing bone pile -- and a persistent, creeping increase in manufacturing costs.

* Some call their bone pile “work-in-process,” “overhead,” “scrap,” or “write-off.”

Learned Thresholds

Initially a “good" (i.e., connected) pin response is learned by the parasitic diode technique from a known good board (KGB), and the test threshold is established (see Figure 3). However, over time, with vendor and batch-to-batch changes, the "good" pin response may drop below the test threshold, causing all boards to fail. A new KGB from the new batch is “learned," the threshold reset, and the process continues. After this happens several times, the threshold may be lowered so far that everything passes, including defects. The only way to realize that discrimination has been lost is to watch for a deliberately injected known fault or to hear feedback from a downstream test station that complains about lower yields from your escapes. Because of the learned threshold process, false pass rates for this technique vary widely, and can become very high.

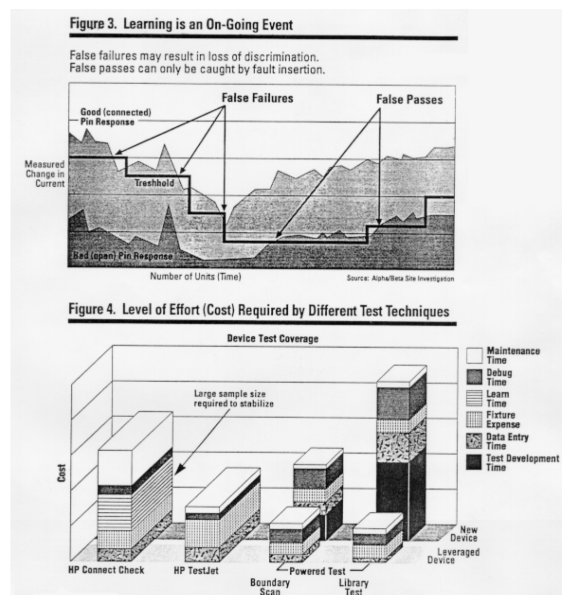


Figure 3. Learning is an On-Going Event

Figure 4. Level of Effort (Cost) Required by Different Test Techniques

Using a learned threshold to distinguish defects results in a significant amount of maintenance and adjustment time after the technique is in production, with a widely variable false pass rate. The tradeoff is in the ability to

achieve some test, where packaging prohibits accessibility to the more reliable Agilent TestJet. Level of Effort A look at the overall level of effort required to implement and maintain the test techniques puts them in perspective. Implementing any test technique requires a typical sequence of efforts, from test development, data entry, and fixturing, to debug and maintenance. Establishing and maintaining learned pass/fail thresholds requires additional time. A critical consideration when implementing Agilent Connect Check or any other parasitic diode technique is the large amount of time required for chronic test maintenance to adjust for component vendor and batch changes, and engineering change orders.

The bar chart in Figure 4 shows the relative time required -- hence costs -- for implementing typical board test measurement techniques. Note that the learn and maintenance steps in Agilent Connect Check (which hold true for any parasitic diode technique) add significantly to the overall cost of using the technique. Even with its larger fixturing cost, Agilent TestJet still provides a much lower overall cost of test. Summary and Conclusion No single test technique is a panacea, curing all testing ills -- not even the newest vectorless tools. Intelligent and appropriate use of vectorless test means understanding the faults most likely to occur on the board being tested, and then minimizing escapes. Escapes are reduced by maximizing test coverage while adjusting for the test technique's inherent limitations.

Agilent TestJet and Agilent Connect Check are two important vectorless test techniques, based on different theoretical models, with unique strengths and limitations. Agilent Connect Check (like all other parasitic diode techniques) should not be used alone, because of its false failure rate and the overall level of effort required to make it effective. Agilent TestJet cannot be used alone when device packaging reduces its effectiveness. Figure 5 summarizes and compares the attributes of Agilent TestJet and Agilent Connect Check.

Agilent TestJet brings unsurpassed test stability, repeatability, and transportability. Agilent TestJet is faster, with an inherently lower false pass rate and overall lower level of effort hence cost - to implement. Agilent Connect Check looks faster to implement initially, but because of learning and maintenance takes more time overall. It looks less costly initially, because it requires a cheaper fixture than Agilent TestJet, but because of its inherently higher false pass rate and implementation level of effort, it costs more overall. At the same time, for appropriate vectorless test applications, it is indispensable. Agilent Connect Check is used when some test is better than none, since it can test packaging inaccessible to Agilent TestJet. Together, these two techniques complement each other, maximizing coverage independent of packaging, device type, and complexity.

With careful consideration of what your unique challenges are, and of the tradeoffs between relevant test coverage, time, and cost, it is possible to find an effective test solution-and keep the bone pile to a minimum -- for your application. For SMT manufacturers, an effective test solution is very likely to include Agilent TestJet and Agilent Connect Check for early, pin-point diagnosis of solder opens, independent of packaging technologies.

Figure 5. Summary and Comparison of Attributes

Attributes	Agilent TestJet	Agilent Connect Check
Dependent measurement parameters	Mechanically specified parameters	Non-specified (variable) parameters
False pass rate	Consistently low	Widely variable
Test threshold	Automatically generated mathematically	Repetitive learning from known good boards

Connectivity issues	Not sensitive	Sensitive; performs better on isolated devices
Engineering change orders	Not sensitive	Requires relearning of threshold
Component variations	Not sensitive	Sensitive
No-clean process	Less sensitive	More sensitive
Fixture	Requires overclamp and probes	Not Required
Information required for test development	XY locations required	Complete topology required